Claims:

Amend claims 1-16 as follows:

Claim 1 **(currently amended)**: A method for debugging a circuit design given ~~with constraining information, the constraining information including~~ a first set of at least one candidate branch, a second set of at least one correction probe, and a third set of at least zero restriction probe, comprising the steps of:

obtaining said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe, whereby the existence of some functional mistake in the circuit design is clearly shown with definite boundaries;

building a representation of the relationships among objects including said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe; and

identifying combinations of behaviors at members of said first set of at least one candidate branch ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe, whereby more accurate information on the location of the functional mistake is derived.

Claim 2 **(original)**: The method of claim 1, wherein said representation of the relationships among objects including said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe is a fourth set of at least one binary decision diagram.

Claim 3 **(original)**: The method of claim 2, wherein an input variable of a member of said fourth set of at least one binary decision diagram corresponds to a member of said first set of at least one candidate branch.

Claim 4 **(currently amended)**: The method of claim 3, wherein said combinations of behaviors at members of said first set of at least one candidate branch ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe are represented as paths that connect the root node to a predetermined leaf node in a member of said fourth set of at least one binary decision diagram.

Claim 5 **(original)**: The method of claim 4, wherein a member of said fourth set of at least one binary decision diagram is ordered and reduced.

Claim 6 **(currently amended)**: The method of claim 5, wherein further comprising the step of:

computing, based on said combinations of behaviors at members of said first set of at least one candidate branch, a ~~likelihood~~ rating for a member of said first set of at least one candidate branch.

Claim 7 **(currently amended)**: The method of claim 6, wherein further comprising the step of:

determining, based on said ~~likelihood~~ rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch must be changed ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 8 **(currently amended)**: The method of claim 6, wherein further comprising the step of:

determining, based on said ~~likelihood~~ rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 9 **(currently amended)**: The method of claim 6, wherein further comprising the step of:

determining, based on said ~~likelihood~~ rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch is never required to be changed ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 10 **(original)**: The method of claim 5, wherein further comprising the step of:

determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch has no impact on whether said circuit design satisfies the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 11 **(currently amended)**: The method of claim 5, wherein further comprising the step of:

determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation

expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 12 **(currently amended)**: The method of claim 4, wherein further comprising the step of:

determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 13 **(currently amended)**: The method of claim 1, wherein further comprising the step of:

determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 14 **(currently amended)**: The method of claim 1, wherein further comprising the step of:

computing a ~~likelihood~~ rating for a member of said first set of at least one candidate branch based on said combinations of behaviors at members of said first set of at least one candidate branch.

Claim 15 **(currently amended)**: The method of claim 14, wherein further comprising the step of:

determining, based on said ~~likelihood~~ rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, ~~such that~~to make said circuit design ~~satisfies~~satisfy the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe.

Claim 16 **(original)**: The method of claim 1, wherein further comprising the step of:

constructing a fifth set of at least one branch cone wherein each input to a member of said fifth set of at least one branch cone corresponds to a member of said first set of at least one candidate branch, whereby said fifth set of at least one branch cone is used for the step of building said representation of the relationships among objects including said circuit design, said first set of at least one candidate

branch, said second set of at least one correction probe, and said third set of at least zero restriction probe.

Claim 17 **(new)**: The method of claim 1, wherein said third set of at least zero restriction probe has one or more members.